NI SC Express

NI PXIe-4330/4331 User Manual

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National Instruments Corporate Headquarters

11500 North Mopac Expressway Austin, Texas 78759-3504 USA Tel: 512 683 0100

Worldwide Offices

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1

Getting Started

The NI PXIe-4330/4331 provides eight simultaneously sampled input channels for interfacing to strain-gage bridges and other Wheatstone-bridge based sensors. These modules have 24-bit resolution and support the following sample rates:

- NI PXIe-4330—up to 25.6 kS/s
- NI PXIe-4331—up to 102.4 kS/s

You can configure all settings on a per channel basis in software. The channels support the following features:

- Connecting sensors of all bridge configurations, including quarter-, half-, and full-bridge.
- Setting the DC voltage excitation between 0.625 V and 10 V.
- Selecting 120 Ω, 350 Ω, and 1 kΩ quarter-bridge completion resistors.
- Programmable bridge offset null and shunt calibration.
- Analog and digital filtering to reject out-of-band signals.
- Remote sense of bridge excitation.

Installation

Refer to the *NI SC Express 4330/4331 Installation Guide and Terminal Block Specifications* for step-by-step software and hardware installation instructions.

Module Specifications

Refer to the *NI PXIe-4330/4331 Specifications* document for module specifications.

Module Accessories and Cables

Refer to the *NI SC Express 4330/4331 Installation Guide and Terminal Block Specifications* document for information about supported accessories and cables.

2

Using the Module

This chapter describes how to connect Wheatstone bridge sensors to the NI PXIe-4330/4331 in quarter-, half-, and full-bridge configurations and for remote sensing. It also provides the I/O connector signal pin assignments of the module.

Connecting Signals

This section includes a brief description of a general Wheatstone bridge and discusses how to connect the signals of supported strain-gage configuration types. It also discusses connecting leads for remote sensing and shunt calibration. Refer to the *NI SC Express 4330/4331 Installation Guide and Terminal Block Specifications* for more signal connection information.

Wheatstone Bridges

Many sensors including strain-gages, load cells, pressure sensors, and torque sensors are based on the concept of a Wheatstone bridge. There are four elements or legs in a Wheatstone bridge. In general, these elements can be resistive or reactive, but in the majority of bridge based sensors the elements are resistive. Most Wheatstone bridge based sensors use all four legs of the bridge as active sensing elements. However, common strain gage configurations include one, two or four active sensing elements. Figure 2-1 shows a resistive Wheatstone bridge circuit diagram.

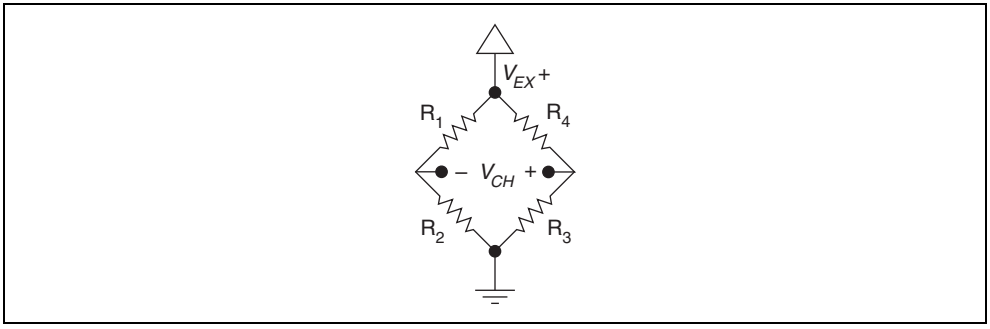


Figure 2-1. Basic Wheatstone Bridge Circuit Diagram

The Wheatstone bridge is the electrical equivalent of two parallel voltage divider circuits. R_1 and R_2 compose one voltage divider circuit, and R_4 and R_3 compose the second voltage divider circuit. The output of a Wheatstone bridge is measured between the middle nodes of the two voltage dividers. A physical phenomena, such as a change in strain or temperature applied to a specimen, changes the resistance of the sensing elements in the Wheatstone bridge, resulting in a bridge output voltage that is proportional to the physical phenomena. The output voltage of the bridge scales with the excitation voltage. However, the ratio of the bridge output (V_{CH}) and the excitation voltage (V_{EX}) remains fixed over variations in excitation voltage, and it is this unitless ratio (V_{CH}/V_{EX}) that is of interest. To accurately measure the ratiometric output of a bridge based sensor both the bridge output voltage (V_{CH}) and the excitation voltage must be known. Determination of the excitation voltage can be accomplished by either using an accurate voltage source or by measuring it. The NI PXIe-4330/4331 uses circuitry that continuously measures the excitation voltage and applies it as a reference to its analog-to-digital converter (ADC). In this way, variations in the excitation voltage are compensated for, and the module returns data as a ratio of the bridge output voltage and the excitation voltage.

Connection Options to Correct for Resistance Errors

The basic Wheatstone bridge in Figure 2-1 shows the excitation voltage impressed directly across the bridge. However, field wiring used to connect sensors to measurement devices have a non-zero resistance, and this resistance can create errors in bridge circuit measurements. The NI PXIe-4330/4331 provides two mechanisms to correct for these errors: remote sensing and shunt calibration.

Remote Sensing

Remote sensing continuously and automatically corrects for errors in excitation leads, and generally is most appropriate for half- and full-bridge sensors. Moreover, its use is most critical in applications that employ long wires and/or small gauge wires, as these have greater resistance. The resistance in the wires that connect the excitation voltage to the bridge causes a voltage drop, which is a source of gain error. The NI PXIe-4330/4331 includes remote sensing to compensate for this gain error. Connect remote sense inputs of the NI PXIe-4330/4331 to the excitation voltage wires of the sensor as close to the bridge circuit as possible. Refer to the full-bridge diagram in Figure 2-2 for an illustration of how to connect remote sense wires.

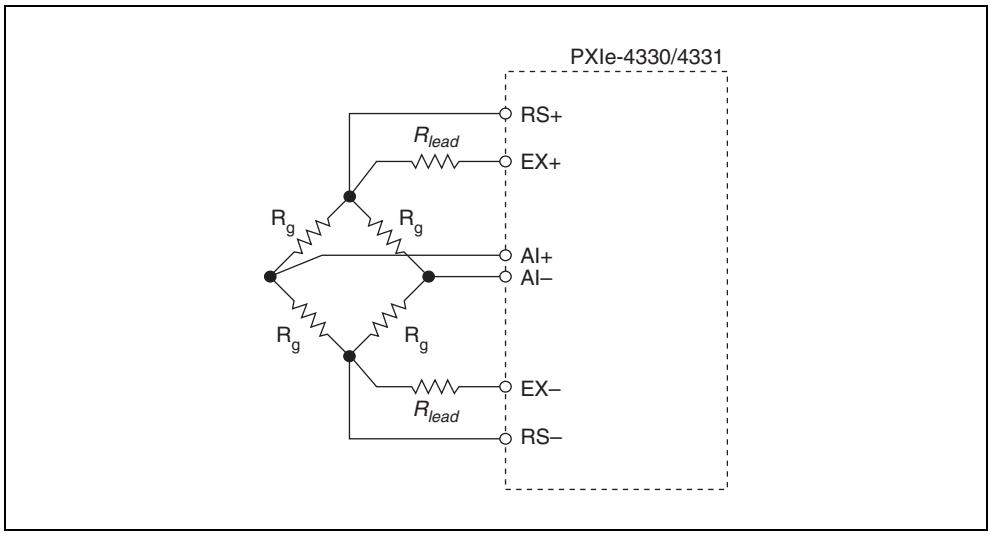


Figure 2-2. Connecting Remote Sense Wires to the NI PXIe-4330/4331

The actual bridge excitation voltage measured at the bridge is smaller than the voltage sourced at the EX+ and EX– connector pins. This reduction in voltage is due to the voltage drop across the excitation lead wire resistance (R_{lead}). If you do not use remote sensing of the actual bridge voltage, the resulting reduction in gain is given by the following equations:

- for half-bridge sensors $\frac{R_{lead}}{R_g}$
- for full-bridge sensors $\frac{2 \cdot R_{lead}}{R_g}$

If you connect the remote sense signals directly to the bridge resistors, the NI PXIe-4330/4331 senses the actual bridge voltage using high-impedance RS leads and eliminates the gain errors caused by the resistance of the EX+ and EX– leads.

Shunt Calibration

Shunt calibration can correct for errors from the resistance of both the excitation wiring and wiring in the individual resistors of the bridge. Remote sensing corrects for resistances from the EX leads on the NI PXIe-4330/4331 to the sensor, and shunt calibration corrects for these errors and for errors caused by wire resistance within an arm of the bridge. Shunt calibration is most useful with three-wire quarter-bridge sensors because there may be significant resistance in the wiring to the sensor and remote sense can not be used. Refer to Figure 2-4 for a diagram of this setup. The NI PXIe-4330/4331 shunt calibration circuitry consists of precision resistors and software-controlled switches. The shunt calibration resistors are built into the module and referenced to EX–. Refer to the software help for information about enabling the shunt calibration resistors on the NI PXIe-4330/4331. Shunt calibration involves simulating the input of strain by changing the resistance of an arm in the bridge by some known amount. This is accomplished by shunting, or connecting, a large resistor of known value across one arm of the bridge, creating a known change in the bridge output. You can then measure the output of the bridge and compare it to the expected bridge output value. You can use the results to correct gain errors in the entire measurement path, or to simply verify general operation to gain confidence in the setup.

Strain Gage Sensor Configurations

This section describes the configurations and signal connection of various supported strain-gage configuration types.

Quarter-Bridge Type I

This section provides information for the quarter-bridge strain-gage configuration type I. The quarter-bridge type I measures either axial or bending strain. Figure 2-3 shows how to position a strain-gage resistor in an axial and bending configuration. Figure 2-4 shows the quarter-bridge type I circuit wiring diagram.

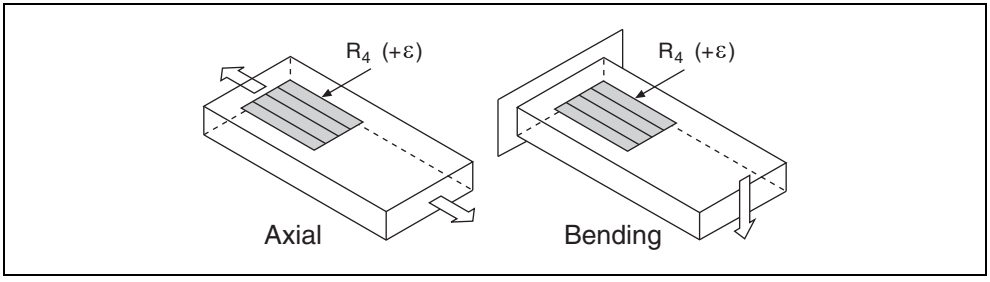


Figure 2-3. Quarter-Bridge Type I Measuring Axial and Bending Strain

A quarter-bridge type I configuration has the following characteristics:

- A single active strain-gage element is mounted in the principal direction of axial or bending strain.

- A passive quarter-bridge completion resistor (R_3) is required in addition to half-bridge completion resistors (R_1 and R_2). All of these resistors are provided by the NI PXIe-4330/4331 module.
- Sensitivity ~ 0.5 µV/V per µε, for GF = 2.0.

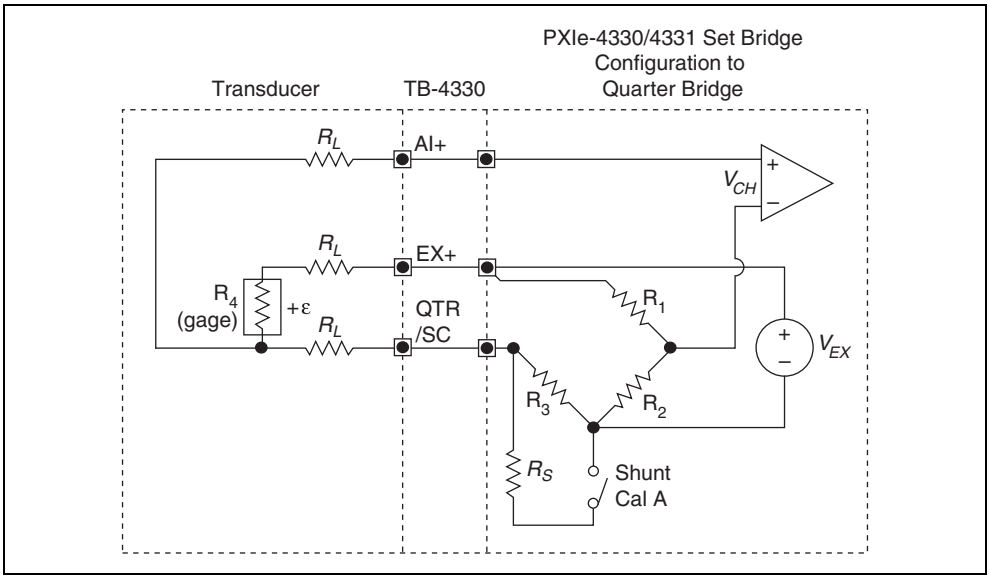


Figure 2-4. Quarter-Bridge I Circuit Diagram

The following symbols apply to the circuit diagram and equations:

- R_1 and R_2—Half-bridge completion resistors located inside the NI PXIe-4330/4331.
- R_3—Quarter-bridge completion resistor located inside the NI PXIe-4330/4331.
  - R_3 must be equal to the nominal resistance of the active gage (R_4).
- R_S—Shunt calibration resistor located inside the NI PXIe-4330/4331.
- R_4—Active element measuring tensile strain (+ε). You provide this element.
- R_L—Lead resistance. The resistance in the EX+ and QTR/SC field wiring should match.
- *GF*—Gage Factor, specified by the gage manufacturer.
- V_{CH}—Measured voltage of the bridge.
- V_{EX}—Excitation voltage provided by the NI PXIe-4330/4331.
- V_r—Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left(\frac{V_{CH}(strained) - V_{CH}(unstrained)}{V_{EX}} \right)$$

Note The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4330/4331.

To convert module readings to strain use the following equation:

$$strain(\varepsilon) = \frac{-4V_r}{GF(1+2V_r)}$$

To compensate for lead resistance errors shunt calibration should be used.

Quarter-Bridge Type II

This section provides information for the quarter-bridge strain-gage configuration type II. The quarter-bridge type II configuration measures either axial or bending strain. Figure 2-5 shows how to position a strain-gage resistor in an axial and bending configurations. Figure 2-6 shows the quarter-bridge type II circuit wiring diagram.

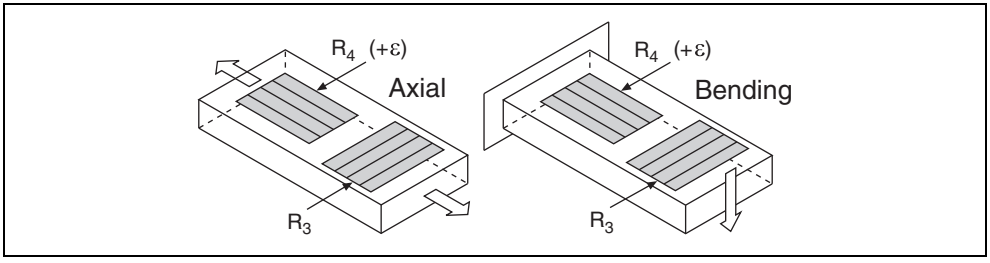


Figure 2-5. Quarter-Bridge Type II Measuring Axial and Bending Strain

A quarter-bridge type II has the following characteristics:

- One active strain-gage element and one passive quarter-bridge element (dummy gage) used for temperature compensation. The active element (R_4) is mounted in the direction of axial or bending strain. The dummy gage (R_3) is mounted in close thermal contact with the strain specimen but not bonded to the specimen, and is usually mounted perpendicular to the principal axis of strain.
- Completion resistors (R_1 and R_2) provide half-bridge completion. These resistors are provided by the NI PXIe-4330/4331 module.
- Sensitivity ~ 0.5 µV/V per µε, for GF = 2.0.

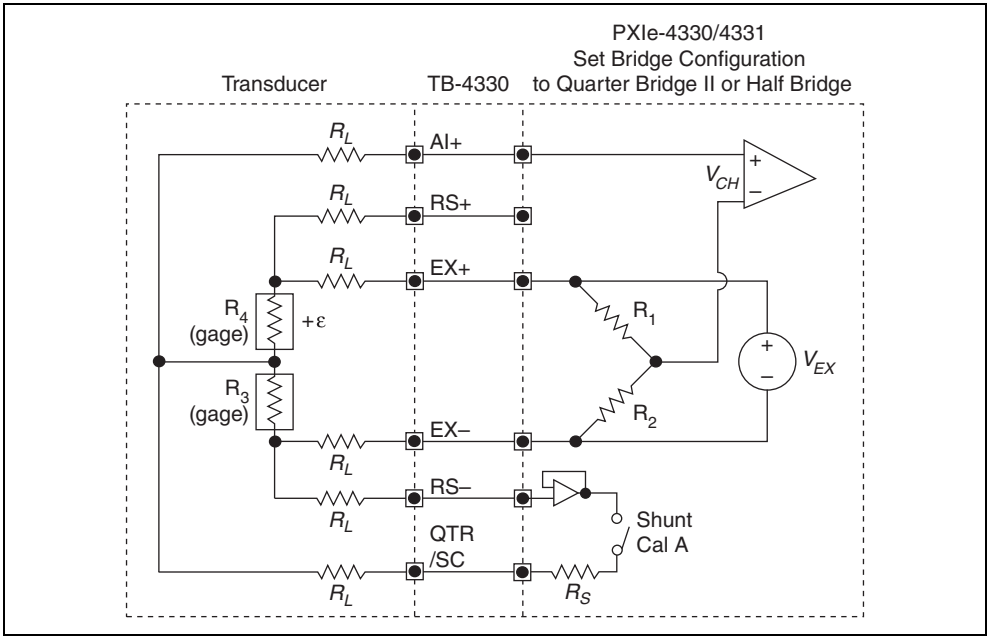


Figure 2-6. Quarter-Bridge II Circuit Diagram

The following symbols apply to the circuit diagram and equations:

- R_1 and R_2—Half-bridge completion resistors located inside the NI PXIe-4330/4331.
- R_3—Quarter-bridge completion resistor located in close proximity to the active gage.
  - R_3 must be equal to the nominal resistance of the active gage (R_4).
- R_S—Shunt calibration resistor located inside the NI PXIe-4330/4331.
- R_4—Active element measuring tensile strain (+ε).
- R_L—Lead resistance.
- GF—Gage Factor, specified by the gage manufacturer.
- V_{CH}—Measured voltage of the bridge.
- V_{EX}—Excitation voltage provided by the NI PXIe-4330/4331.
- V_r—Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left(\frac{V_{CH}(strained) - V_{CH}(unstrained)}{V_{EX}}\right)$$

Note The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4330/4331.

To convert module readings to strain use the following equation:

$$strain(\varepsilon) = \frac{-4V_r}{GF(1+2V_r)}$$

Half-Bridge Type I

This section provides information for the half-bridge strain-gage configuration type I. The half-bridge type I measures either axial or bending strain. Figure 2-7 shows how to position strain-gage resistors in an axial and bending configurations. Figure 2-8 shows the half-bridge type I circuit wiring diagram.

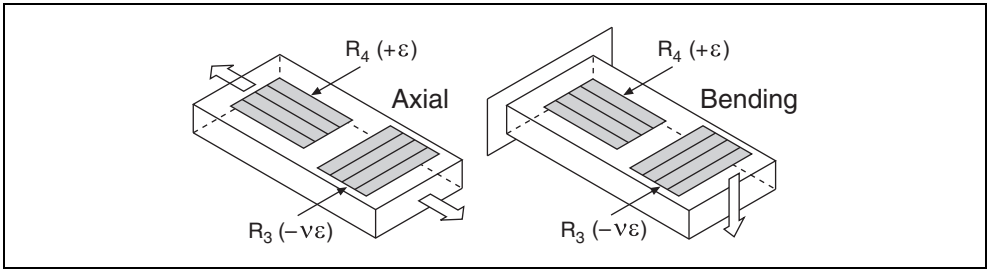


Figure 2-7. Half-Bridge Type I Measuring Axial and Bending Strain

A half-bridge type I has the following characteristics:

- Two active strain-gage elements. One strain-gage element is mounted in the direction of axial strain while the other acts as a Poisson gage and is mounted perpendicular to the principal axis of strain.
- Half-bridge completion resistors (R_1 and R_2) are provided by the NI PXIe-4330/4331.
- Sensitive to both axial and bending strain.
- Sensitivity ~ 0.65 μV/V per με, for GF = 2.0.

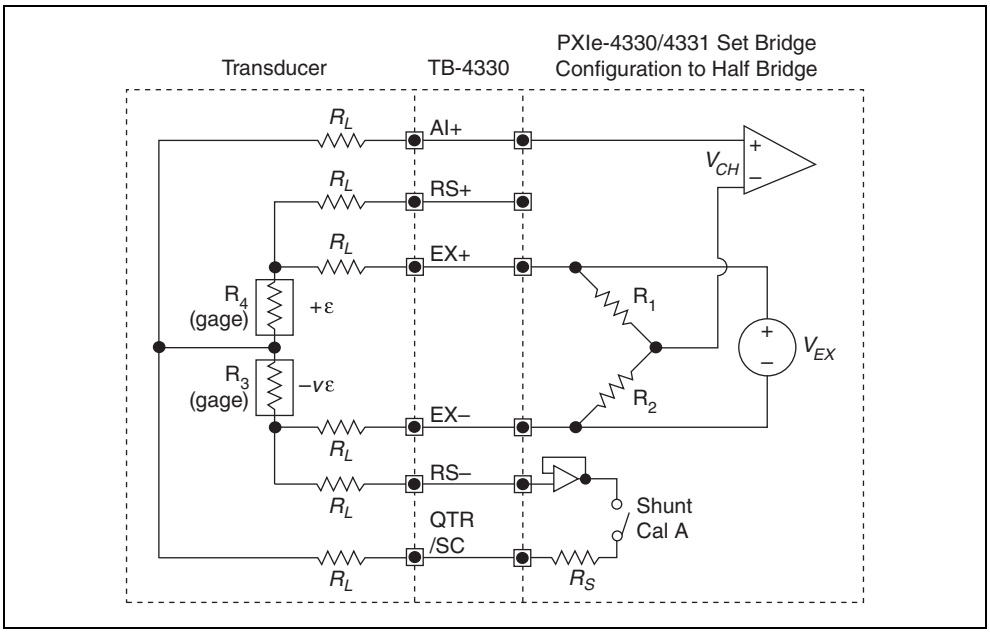


Figure 2-8. Half-Bridge Type I Circuit Diagram

The following symbols apply to the circuit diagram and equations:

- R_1 and R_2—Half-bridge completion resistors located inside the NI PXIe-4330/4331.
- R_3—Active element measuring compression from Poisson effect ($-\nu\varepsilon$).
- R_S—Shunt calibration resistor located inside the NI PXIe-4330/4331.
- R_4—Active element measuring tensile strain ($+\varepsilon$).
- R_L—Lead resistance.
- *GF*—Gage Factor, specified by the gage manufacturer.
- ν—Poisson's ratio, defined as the negative ratio of transverse strain to axial strain (longitudinal) strain. Poisson's ratio is a material property of the specimen you are measuring.
- V_{CH}—Measured voltage of the bridge.
- V_{EX}—Excitation voltage provided by the NI PXIe-4330/4331.
- V_r—Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left(\frac{V_{CH}\ (strained) - V_{CH}\ (unstrained)}{V_{EX}} \right)$$

Note The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4330/4331.

To convert module readings to strain use the following equation:

$$strain(\varepsilon) = \frac{-4V_r}{GF[(1+\nu)-2V_r(\nu-1)]}$$

Half-Bridge Type II

This section provides information for the half-bridge strain-gage configuration type II. The half-bridge type II only measures bending strain. Figure 2-9 shows how to position strain-gage resistors in a bending configuration. Figure 2-10 shows the half-bridge type II circuit wiring diagram.

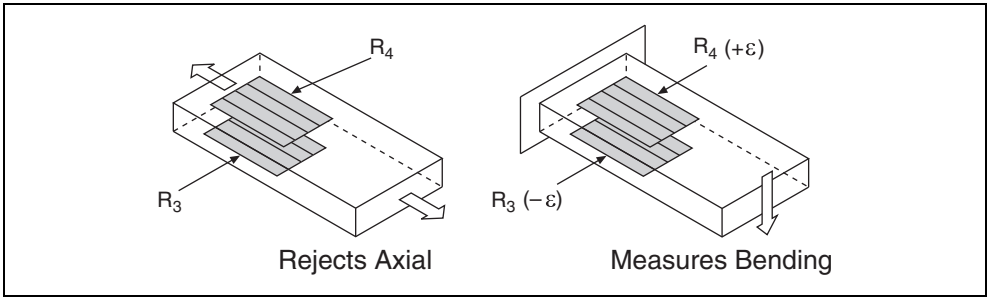


Figure 2-9. Half-Bridge Type II Rejecting Axial and Measuring Bending Strain

A half-bridge type II configuration has the following characteristics:

- Two active strain-gage elements. One strain-gage element is mounted in the direction of bending strain on one side of the strain specimen (top) while the other is mounted in the direction of bending strain on the opposite side (bottom).
- Half-bridge completion resistors (R_1 and R_2) are provided by the NI PXIe-4330/4331.
- Sensitive to bending strain.
- Rejects axial strain.
- Sensitivity ~ 1 μV/V per με, for GF = 2.0.

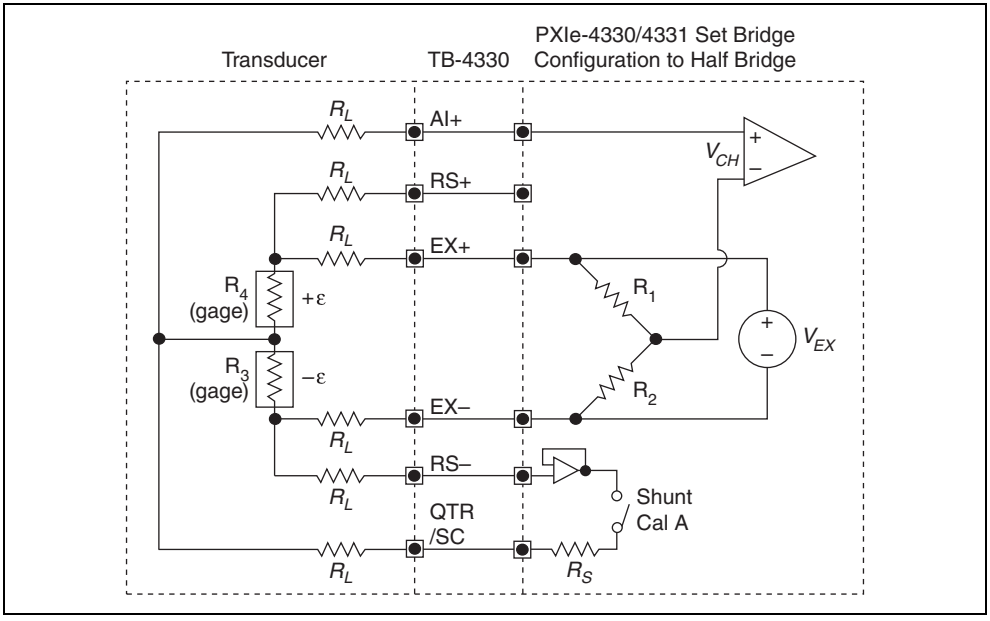


Figure 2-10. Half-Bridge Type II Circuit Diagram

The following symbols apply to the circuit diagram and equations:

- R_1 and R_2—Half-bridge completion resistors located inside the NI PXIe-4330/4331.
- R_3—Active element measuring compressive strain (–ε).
- R_s—Shunt calibration resistor located inside the NI PXIe-4330/4331.
- R_4—Active element measuring tensile strain (+ε).
- R_L—Lead resistance.
- *GF*—Gage Factor, specified by the gage manufacturer.
- V_{CH}—Measured voltage of the bridge.
- V_{EX}—Excitation voltage provided by the NI PXIe-4330/4331.

V_r—Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left(\frac{V_{CH}(strained) - V_{CH}(unstrained)}{V_{EX}} \right)$$

Note The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4330/4331.

To convert module readings to strain use the following equation:

$$strain\ (\varepsilon) = \frac{-2V_r}{GF}$$

Full-Bridge Type I

This section provides information for the full-bridge strain-gage configuration type I. The full-bridge type I only measures bending strain. Figure 2-11 shows how to position strain-gage resistors in a bending configuration. Figure 2-12 shows the full-bridge type I circuit wiring diagram.

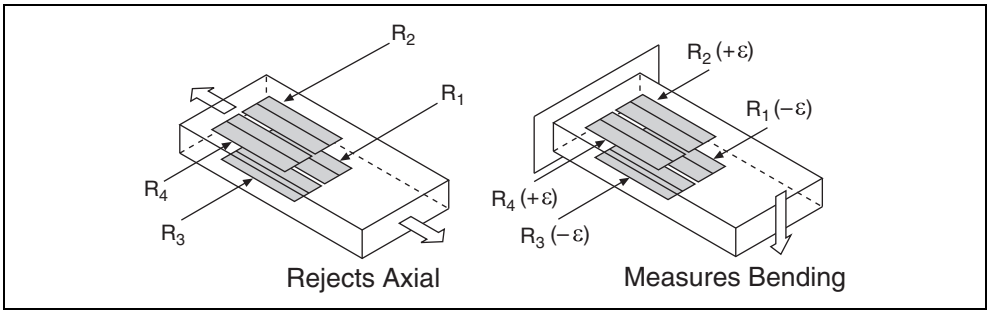


Figure 2-11. Full-Bridge Type I Rejecting Axial and Measuring Bending Strain

A full-bridge type I configuration has the following characteristics:

- Four active strain-gage elements. Two strain-gage elements are mounted in the direction of bending strain on one side of the strain specimen (top) while the other two are mounted in the direction of bending strain on the opposite side (bottom).
- Highly sensitive to bending strain.
- Rejects axial strain.
- Sensitivity ~ 2 μV/V per με, for GF = 2.0.

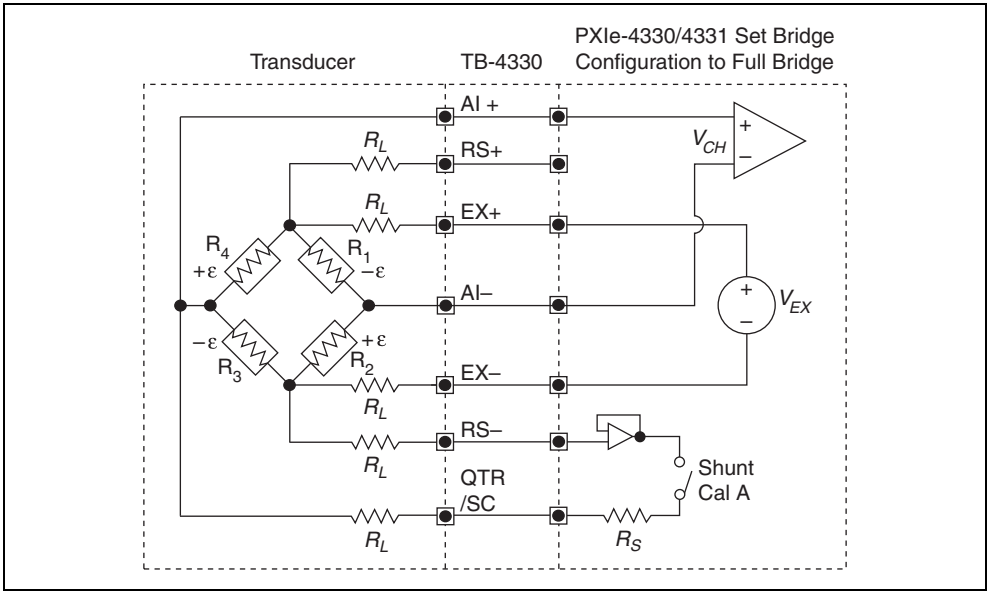


Figure 2-12. Full-Bridge Type I Circuit Diagram

The following symbols apply to the circuit diagram and equations:

- R_1—Active element measuring compressive strain (–ε).
- R_2—Active element measuring tensile strain (+ε).
- R_3—Active element measuring compressive strain (–ε).
- R_4—Active element measuring tensile strain (+ε).
- R_s — Shunt calibration resistor located inside the NI PXIe-4330/4331.
- R_L—Lead resistance.
- *GF*—Gage Factor, specified by the gage manufacturer.
- V_{CH}—Measured voltage of the bridge.
- V_{EX}—Excitation voltage provided by the NI PXIe-4330/4331.
- V_r—Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left(\frac{V_{CH}(strained) - V_{CH}(unstrained)}{V_{EX}} \right)$$

Note The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4330/4331.

To convert module readings to strain use the following equation:

$$strain\ (\varepsilon) = \frac{-V_r}{GF}$$

Full-Bridge Type II

This section provides information for the full-bridge type II strain-gage configuration. The full-bridge type II only measures bending strain. Figure 2-13 shows how to position strain-gage resistors in a bending configuration. Figure 2-14 shows the full-bridge type II circuit wiring diagram.

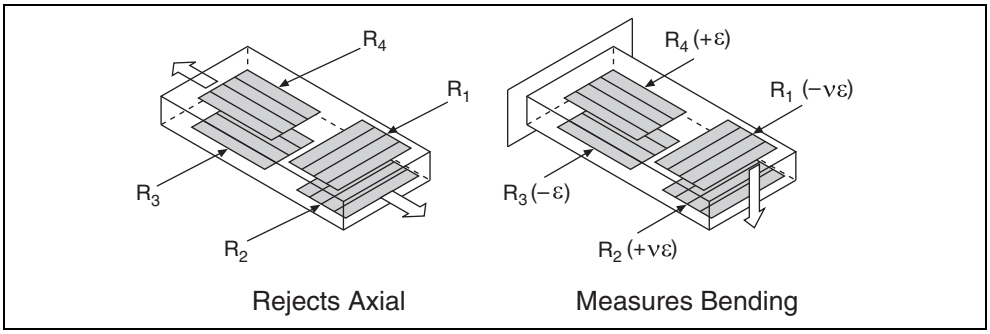


Figure 2-13. Full-Bridge Type II Rejecting Axial and Measuring Bending Strain

A full-bridge type II configuration has the following characteristics:

- Four active strain-gage elements. Two are mounted in the direction of bending strain with one on one side of the strain specimen (top) and the other on the opposite side (bottom). The other two act together as a Poisson gage and are mounted transverse (perpendicular) to the principal axis of strain with one on one side of the strain specimen (top) and the other on the opposite side (bottom).
- Rejects axial strain.
- Sensitivity ~ 1.3 μV/V per με, for GF = 2.0.

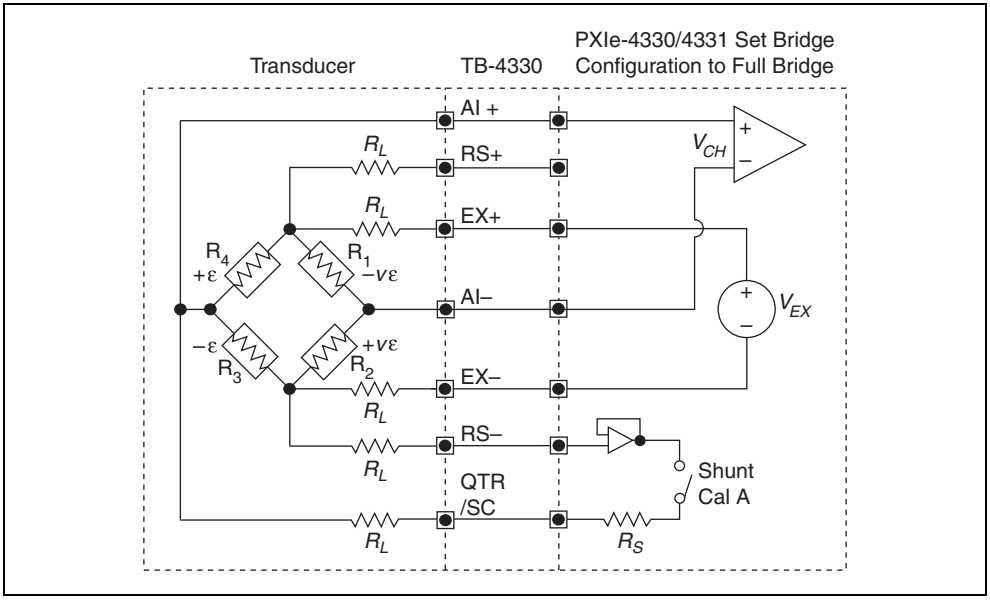


Figure 2-14. Full-Bridge Type II Circuit Diagram

The following symbols apply to the circuit diagram and equations:

- R_1—Active element measuring compressive Poisson effect ($-\nu\varepsilon$).
- R_2—Active element measuring tensile Poisson effect ($+\nu\varepsilon$).
- R_3—Active element measuring compressive strain ($-\varepsilon$).
- R_4—Active element measuring tensile strain ($+\varepsilon$).
- R_s — Shunt calibration resistor located inside the NI PXIe-4330/4331.
- R_L — Lead resistance.
- *GF*—Gage Factor, specified by the gage manufacturer.
- ν—Poisson's ratio, defined as the negative ratio of transverse strain to axial strain (longitudinal) strain. Poisson's ratio is a material property of the specimen you are measuring.
- V_{CH}—Measured voltage of the bridge.
- V_{EX}—Excitation voltage provided by the NI PXIe-4330/4331.
- V_r—Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left(\frac{V_{CH}(strained) - V_{CH}(unstrained)}{V_{EX}}\right)$$

Note The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4330/4331.

To convert module readings to strain use the following equation:

$$strain(\varepsilon) = \frac{-2V_r}{GF(1+\nu)}$$

Full-Bridge Type III

This section provides information for the full-bridge strain-gage configuration type III. The full-bridge type III only measures axial strain. Figure 2-15 shows how to position strain-gage resistors in an axial configuration. Figure 2-16 shows the full-bridge type III circuit wiring diagram.

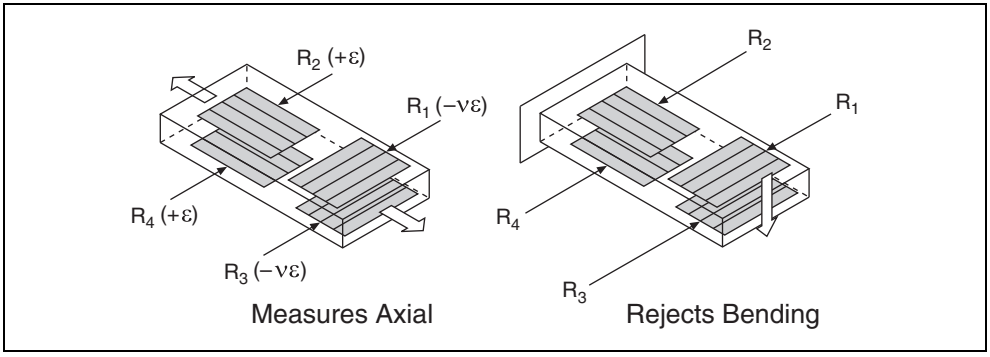


Figure 2-15. Full-Bridge Type III Measuring Axial and Rejecting Bending Strain

A full-bridge type III configuration has the following characteristics:

- Four active strain-gage elements. Two strain-gage elements are mounted in the direction of axial strain with one on one side of the strain specimen (top) while the other is on the opposite side (bottom). The other two act together as a Poisson gage and are mounted transverse (perpendicular) to the principal axis of strain with one on one side of the strain specimen (top) and the other on the opposite side (bottom).
- Rejects bending strain.
- Sensitivity ~ 1.3 μV/V per με, for GF = 2.0.

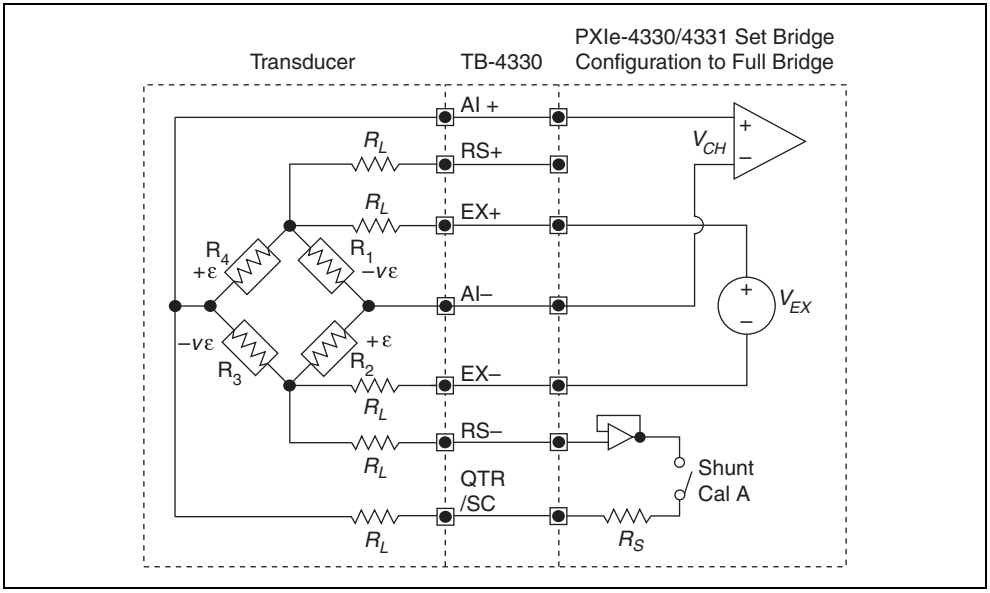


Figure 2-16. Full-Bridge Type III Circuit Diagram

The following symbols apply to the circuit diagram and equations:

- R_1—Active element measuring compressive Poisson effect (–νε).
- R_2—Active element measuring tensile strain (+ε).
- R_3—Active element measuring compressive Poisson effect (–νε).
- R_4—Active element measuring the tensile strain (+ε).
- R_L—Lead resistance.
- *GF*—Gage Factor, specified by the gage manufacturer.
- ν—Poisson's ratio, defined as the negative ratio of transverse strain to axial strain (longitudinal) strain. Poisson's ratio is a material property of the specimen you are measuring.
- R_s—Shunt calibration resistor located inside the NI PXIe-4330/4331.
- V_{CH}—Measured voltage of the bridge.
- V_{EX}—Excitation voltage provided by the NI PXIe-4330/4331.
- V_r—Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left(\frac{V_{CH}(strained) - V_{CH}(unstrained)}{V_{EX}}\right)$$

Note The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4330/4331.

To convert module readings to strain use the following equation:

$$strain(\varepsilon) = \frac{-2V_r}{GF[(\nu + 1) - V_r(\nu - 1)]}$$

Force, Pressure, and Torque Sensor Configurations

The NI PXIe-4330/4331 can be used with force sensors (such as load cells), pressure sensors, or torque sensors that have the following characteristics:

- Wheatstone bridge based[1]
- Unamplified mV/V or V/V output[2]

These sensors typically use a full-bridge configuration with a 350 Ω nominal bridge resistance, but other configurations and nominal bridge resistances can be used. Figure 2-17 shows the force, pressure, torque sensor circuit diagram.

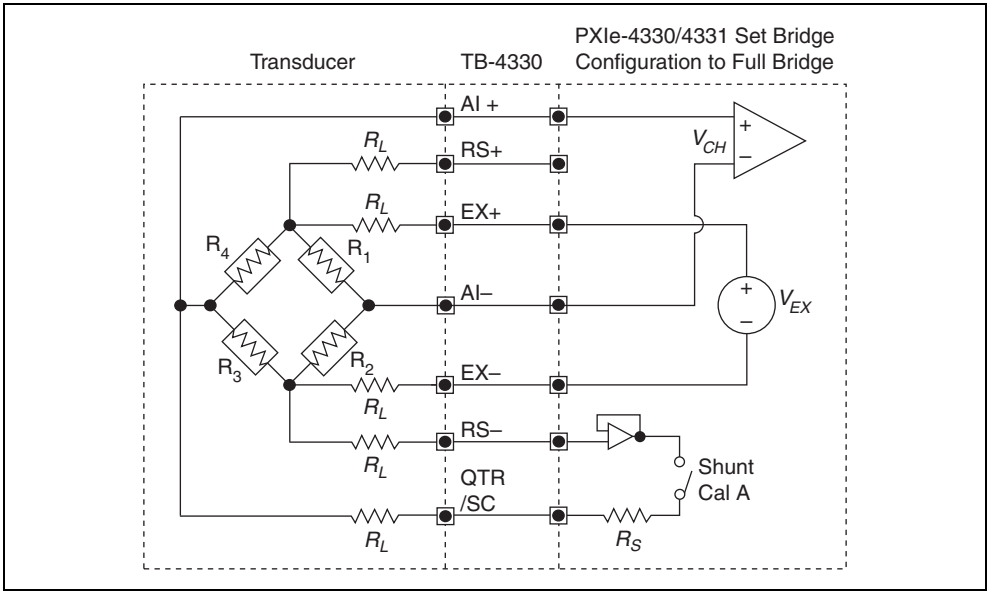


Figure 2-17. Force, Pressure, and Torque Sensor Circuit Diagram

[1] Sensors that measure force, pressure, or torque through other means (for example, piezoelectric force sensors) cannot be used with the NI PXIe-4330/4331.

[2] Sensors that contain a built-in voltage or current amplifier cannot be used with the NI PXIe-4330/4331.

The following symbols apply to the circuit diagram and equations:

- R_1 through R_4—Active elements of the bridge, located inside the sensor.
- R_s—Shunt calibration resistor located inside the NI PXIe-4330/4331.
- R_L—Lead resistance.
- V_{CH} —Measured voltage (sensor output).
- V_{EX}—Excitation voltage provided by the NI PXIe-4330/4331.
- V_r—Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \frac{(V_{CH}\text{ (under load)} - V_{CH}\text{ (no load)})}{V_{EX}}$$

Note The ratio of the bridge output voltage and the excitation voltage is calculated internally on the NI PXIe-4330/4331.

Converting module readings to physical force, pressure, or torque readings can be performed using linear, table, or polynomial scaling.

In NI-DAQmx, linear scaling for bridge-based force, pressure, and torque sensors is done based on two points which are specified as pairs of corresponding physical and electrical values: ($electrical_1$, $physical_1$) and ($electrical_2$, $physical_2$). These should be based on the calibration certificate of the sensor, if one is available; otherwise, they can be based on the specifications or data sheet of the sensor. Any two points can be used, assuming that they are far enough apart to accurately determine the slope of the linear scaling equation. For example:

- $physical_1$—The zero point of the sensor: zero force, pressure, or torque.
- $electrical_1$—The electrical output corresponding to the zero point of the sensor, in mV/V or V/V.
- $physical_2$—The maximum physical reading of the sensor, or capacity: maximum load, pressure, or torque.
- $electrical_2$—The electrical output corresponding to the maximum physical reading of the sensor, in mV/V or V/V.

Note Some sensor calibration certificates specify the electrical output in mV or V, not mV/V or V/V. If this is the case, divide the specified electrical output by the excitation voltage at which the calibration was performed.

The two-point linear conversion uses the following equations:

$$m = \frac{physical_1 - physical_2}{electrical_1 - electrical_2}$$

$$b = physical_1 - m \times electrical_1$$

$$physical\ reading = m \times V_r + b$$

If offset nulling (bridge balancing) is used to compensate for offset, then the zero point of the sensor can be assumed to output exactly 0 V/V, simplifying these equations:

$$m = \frac{physical_2}{electrical_2}$$

$$physical\ reading = m \times V_r$$

When the calibration certificate of the sensor provides a table of more than two calibration points or a polynomial expression, table or polynomial scaling can produce more accurate results by compensating for non-linearity in the response of the sensor. Table scaling requires providing NI-DAQmx with a set of electrical values and corresponding physical values. Polynomial scaling requires providing NI-DAQmx with the forward and reverse coefficients of a polynomial representing the response of the sensor. If you only know one set of coefficients, you can use the DAQmx Compute Reverse Polynomial Coefficients VI/function to determine the other set.

Common-Mode Voltage Considerations

The NI PXIe-4330/4331 supports common-mode voltages between ±2 V. The majority of full-bridge sensors are balanced between the upper and lower arms of the bridge, resulting in a common-mode voltage equal to one-half the excitation voltage when connected to a single-ended excitation voltage or 0 V when connected to a balanced differential excitation voltage. Since the NI PXIe-4330/4331 has a balanced differential excitation voltage source, the common-mode voltage for balanced sensors is equal to 0 V. However, some full-bridge sensors are unbalanced between the upper and lower arms. Common-mode imbalances are often given as a voltage relative to a single-ended voltage excitation source. To convert a common-mode voltage that is specified relative to a single-ended excitation to a common-mode voltage driven by a balanced differential excitation use the following equation:

$$V_{cm} = \frac{V_{ex}}{2} \times (2r - 1)$$

Where r is the ratio of the common-mode voltage of the sensor divided by the excitation, as listed in sensor specifications.

For instance, if a sensor is specified to have a 3 V common mode voltage with a 10 V single-ended excitation, r is equal to 0.3, resulting in a common-mode voltage of –2 V when connected to a balanced differential 10 V excitation voltage supply. For this case –2 V is within the common-mode range of the NI PXIe-4330/4331. If the common-mode voltage was outside of the range of the NI PXIe-4330/4331, it would be necessary to reduce the excitation voltage to a level that results in a common-mode voltage that is within range. To find the maximum excitation voltage that meets this criterion, solve the following equation, setting V_{cm} equal to –2 V if $r < 0.5$ or setting V_{cm} equal to 2 V if $r > 0.5$.

$$V_{ex} = \frac{2(V_{cm})}{2r - 1}$$

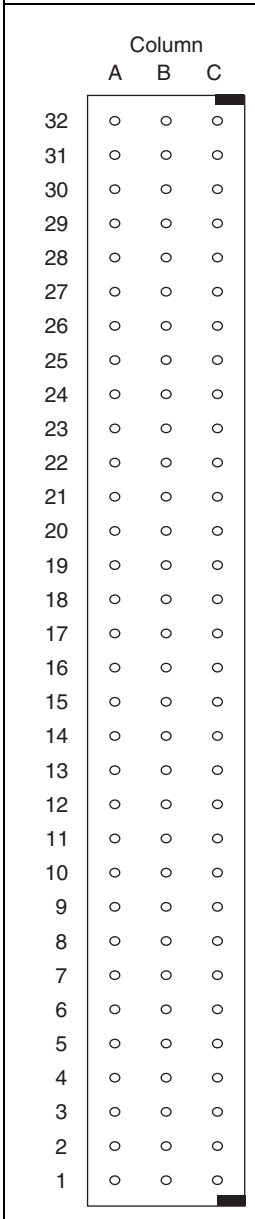
Shielding and Grounding Considerations

Note For proper electromagnetic compatibility (EMC) performance, use shielded wire and connect the shield to the chassis ground.

Module Pinout

This is the pinout represented on the front connector of the NI PXIe-4330/4331. Refer to the *I/O Connector Signal Description* section for definitions of each signal. Refer to the terminal block installation guide for signal locations on the terminal block.

Table 2-1. Front Connector Signal Pin Assignments

Front Connector Diagram	Pin Number	Column A	Column B	Column C	Channel
	32	AIGND	EX+	AI+	0
	31	QTR/SC	EX–	AI–	
	30	QTR/SC	RS–	RS+	
	29	AIGND	EX+	AI+	1
	28	QTR/SC	EX–	AI–	
	27	QTR/SC	RS–	RS+	
	26	AIGND	EX+	AI+	2
	25	QTR/SC	EX–	AI–	
	24	QTR/SC	RS–	RS+	
	23	AIGND	EX+	AI+	3
	22	QTR/SC	EX–	AI–	
	21	QTR/SC	RS–	RS+	
	20	DGND	T0+	T1+	No Channel
	19	T3+	T0–	T1–	
	18	T3–	T2–	T2+	
	17	DGND	T4+	T5+	
	16	T7+	T4–	T5–	
	15	T7–	T6–	T6+	
	14	AIGND	EX+	AI+	4
	13	QTR/SC	EX–	AI–	
	12	QTR/SC	RS–	RS+	
	11	AIGND	EX+	AI+	5
	10	QTR/SC	EX–	AI–	
	9	QTR/SC	RS–	RS+	
	8	AIGND	EX+	AI+	6
	7	QTR/SC	EX–	AI–	
	6	QTR/SC	RS–	RS+	
	5	AIGND	EX+	AI+	7
	4	QTR/SC	EX–	AI–	
	3	QTR/SC	RS–	RS+	
	2	RSVD	DGND	RSVD	No Channel
	1	RSVD	RSVD	RSVD	

RSVD is reserved

I/O Connector Signal Description

Table 2-2 describes the signals found on the I/O connector.

Table 2-2. I/O Connector Signal Descriptions

Signal Names	Direction	Description
AIGND	—	Analog Input Ground
AI<0..7>+, AI<0..7>–	Input	Analog Input Channels 0 to 7—AI+ and AI– are the positive and negative inputs of the differential analog input.
QTR/SC<0..7>	—	These pins provide the connection point for quarter-bridge completion and shunt calibration.
EX<0..7>+, EX<0..7>–	Output	Provides the differential bridge excitation voltage.
RS<0..7>+, RS<0..7>–	Input	Remote sense input. The remote sense pins sense the actual voltage applied to the bridge.
T<0..7>+	Input/Output	TEDS sensor digital communication lines.
T<0..7>–	—	Negative reference for TEDS communication. Internally connected to the module digital ground.
RSVD	—	These pins are reserved for communication with the accessory.
DGND	—	Digital ground—these pins supply the reference for module digital signals and are connected to the module digital ground.

NI PXIe-4330/4331 Block Diagram

Figure 2-18 shows the analog input circuitry block diagram of the NI PXIe-4330/4331.The programmable excitation block provides the excitation voltage for the bridge or sensor. The voltage level is configurable on a per channel basis. This excitation voltage is sensed locally or remotely via the remote sense terminals (RS+ and RS–) and fed back to the ADC (Analog-to-Digital Converter) reference through a programmable gain amplifier. The gain applied when sensing the excitation voltage is automatically selected based on the selected excitation voltage level.

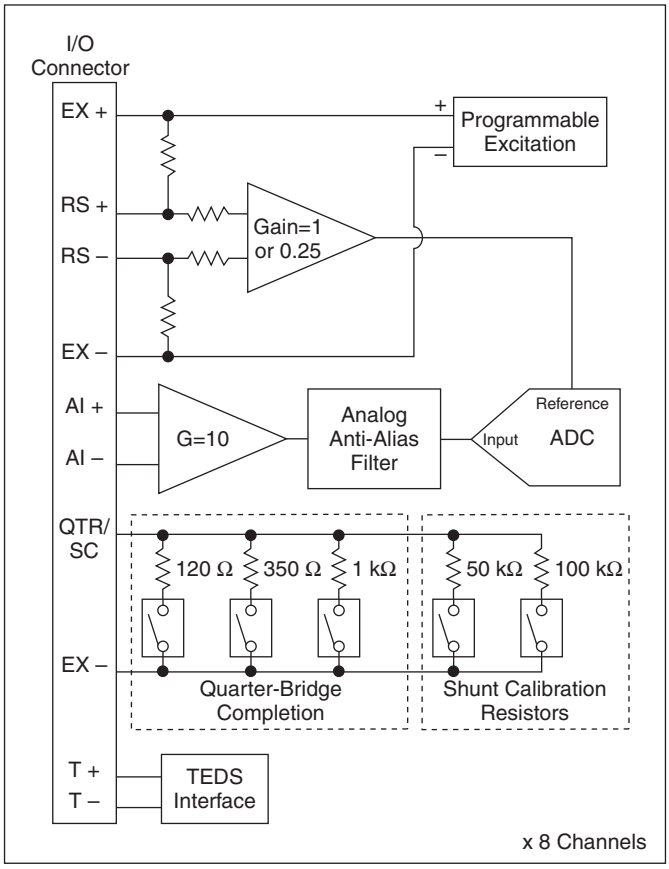


Figure 2-18. NI PXIe-4330/4331 Signal Conditioning Block Diagram

The bridge output voltage is sensed through the AI+ and AI– pins and then amplified and filtered before being fed into the ADC input. The ADC then performs a ratiometric measurement of the input signal versus the reference signal to determine the actual deflection of the bridge or sensor.

The NI PXIe-4330/4331 supports half-, quarter-, and full-bridge measurements. When performing a quarter-bridge measurement, you can configure the NI PXIe-4330/4331 to select between internal 120 Ω, 350 Ω, and 1 kΩ quarter-bridge completion resistors. In addition, you can enable programmable shunt-calibration resistors, individually or in parallel, to provide three different possible shunt-calibration resistor values.

Each channel also provides a transducer electronic data sheet (TEDS) interface. This interface can read the TEDS information from supported sensors to provide plug and play identification of the sensor and scaling information.

Figure 2-19 shows how the ADCs from each channel are connected through to the PXI Express bus. Data from the ADCs are adjusted in hardware to remove offset and gain errors. Then, if required, the data is filtered and decimated to match the specified acquisition rate. Finally, the data is placed into a FIFO where it is transferred through PCI Express to the host computer memory.

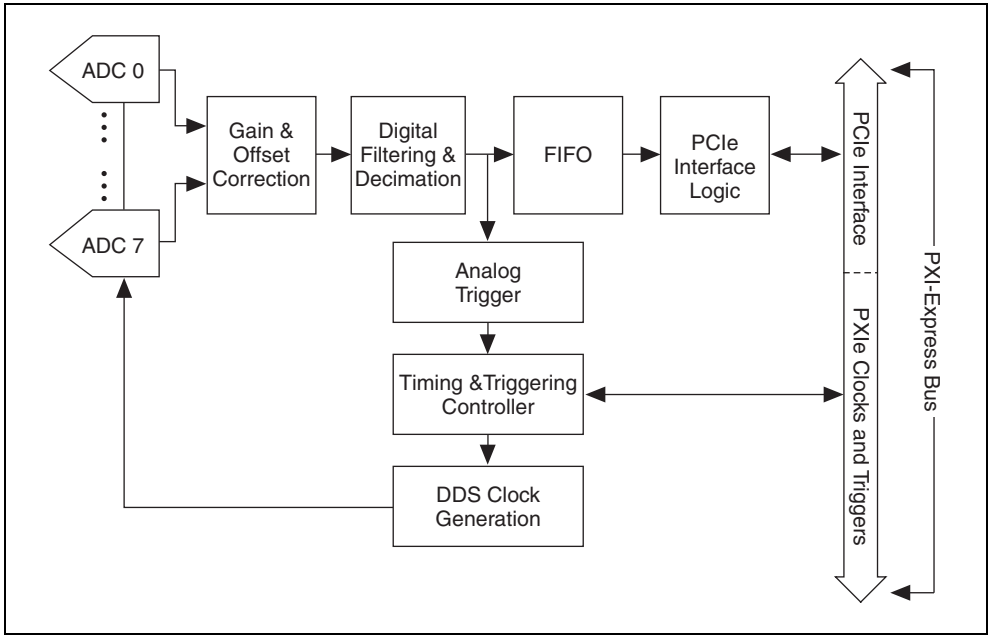


Figure 2-19. NI PXIe-4330/4331 Digital Back End Block Diagram

Timing and triggering of the acquisition is handled by an onboard timing and triggering controller. This controller configures an onboard DDS clock generator to provide an oversample clock to the ADCs in order to acquire data at the specified rate. The DDS clock can be generated either using an onboard oscillator or using the 100 MHz backplane clock provided by PXI Express. Running the DDS clock from the 100 MHz backplane clock allows for synchronization of multiple NI PXIe-4330/4331 modules. In addition to sending and receiving triggers from the PXIe backplane, the NI PXIe-4330/4331 can also be configured to generate an Analog Trigger event from the digitized analog data of its ADCs.

Signal Acquisition Considerations

This section contains information about signal acquisition concepts, including software scaling and equations, Delta-Sigma converters, Nyquist frequency and bandwidth, timing, triggering, and synchronization.

Software Scaling and Equations

After you have acquired the signal of interest, you can scale this measurement to the appropriate units in software. This is done automatically for you in NI-DAQmx using a strain task or strain channel. You also can scale the measurements manually in your application using the measurement-to-strain conversion equations provided in this document for each configuration type. The NI PXIe-4330/4331 also supports measurements for force, pressure, torque, bridge (V/V), and custom voltage with excitation.

Finally, there are voltage-to-strain conversion functions included in LabVIEW and NI-DAQmx. In LabVIEW, the conversion function, Convert Strain Gage Reading VI, is in the **Data Acquisition»Signal Conditioning** subpalette. The prototypes for the NI-DAQ functions, `Strain_Convert` and `Strain_Buf_Convert`, are in the header file `convert.h` for C/C++, and `convert.bas` for Visual Basic.

Refer to the *LabVIEW Measurements Manual* for more information. The names given the strain-gage types in these sections directly correspond to bridge selections in MAX and the LabVIEW Convert Strain Gage Reading VI.

Nyquist Frequency and Nyquist Bandwidth

Any sampling system, such as an ADC, is limited in the bandwidth of the signals it can measure. Specifically, a sampling rate of f_s can represent only signals with frequencies lower than $f_s/2$. This maximum frequency is known as the *Nyquist frequency.* The bandwidth from 0 Hz to the Nyquist frequency is the *Nyquist bandwidth*.

ADC

The NI PXIe-4330/4331 ADCs use a conversion method known as delta-sigma modulation. This approach involves oversampling the input signal at a higher rate and then decimating and filtering the resulting data to achieve the desired sample rate. For example, if the desired data rate is 100 kS/s, each ADC actually samples its input signal at 6.4 MS/s, 64 times the data rate, producing 1-bit samples that are sent to a digital filter. This filter rejects signal components greater than the Nyquist frequency of 50 kHz. The 1-bit, 6.4 MS/s data stream from the ADC contains all of the information necessary to produce 24-bit samples at 100 kS/s. The delta-sigma ADC achieves this conversion from high speed to high resolution with a technique called noise shaping. The ADC adds random noise to the signal so that the resulting quantization noise, although large, is restricted to frequencies above the Nyquist frequency, which is 50 kHz in this case. This noise is not correlated with the input signal and is almost completely rejected by the digital filter.

The resulting output of the filter is a band-limited signal with a large dynamic range. One of the advantages of a delta-sigma ADC is that it uses a 1-bit DAC as an internal reference. As a result, the delta-sigma ADC is free from the differential nonlinearity (DNL) and associated noise inherent in high-resolution ADCs using other conversion techniques.

Analog Input Filters

The NI PXIe-4330/4331 uses a combination of analog and digital filtering to provide an accurate representation of in-band signals while rejecting out-of-band signals. The filters discriminate between signals based on the frequency range, or bandwidth, of the signal. The three important bandwidths to consider are the passband, the stopband, and the alias-free bandwidth.

The NI PXIe-4330/4331 accurately represents signals within the passband, as quantified primarily by passband flatness and phase nonlinearity. All signals that appear in the alias-free bandwidth are either unaliased signals or signals that have been filtered by at least the amount of the stopband rejection.

Anti-Alias Filters

A digitizer or ADC might sample signals containing frequency components above the Nyquist limit. The undesirable effect of the digitizer modulating out-of-band components into the Nyquist bandwidth is aliasing. The greatest danger of aliasing is that you cannot determine whether aliasing occurred by looking at the ADC output. If an input signal contains several frequency components or harmonics, some of these components might be represented correctly while others contain aliased artifacts.

Lowpass filtering to eliminate components above the Nyquist frequency either before or during the digitization process can guarantee that the digitized data set is free of aliased components. The NI PXIe-4330/4331 modules employ both digital and analog lowpass filters to achieve this protection.

The NI PXIe-4330/4331 modules include an oversampled architecture and sharp digital filters with cut-off frequencies that track the sampling rate. Thus, the filter automatically adjusts to follow the Nyquist frequency. Although the digital filter eliminates almost all out-of-band components, it is still susceptible to aliases from certain narrow frequency bands located at frequencies far above the sampling rate. These frequencies are referred to as the ADC alias holes.

In addition to the digital filtering, the NI PXIe-4330/4331 modules feature a fixed-frequency analog filter. The analog filter removes high-frequency components in the analog signal path before they reach the ADC. This filtering addresses the possibility of high-frequency aliasing from the narrow bands that are not covered by the digital filter.

While the frequency response of the digital filter directly scales with the sample rate, the analog filter –3dB point is fixed. The NI PXIe-4330/4331 automatically adjusts its oversample rate to maintain a high level of alias protection regardless of the current sampling rate.

Passband

The signals within the passband have frequency-dependent gain or attenuation. The small amount of variation in gain with respect to frequency is called the passband flatness. The digital filters of the NI PXIe-4330/4331 adjust the frequency range of the passband to match the sample rate. Therefore, the amount of gain or attenuation at a given frequency depends on the sample rate.

Stopband

The filter significantly attenuates all signals above the stopband frequency. The primary goal of the filter is to prevent aliasing. Therefore, the stopband frequency scales precisely with the sample rate. The stopband rejection is the minimum amount of attenuation applied by the filter to all signals with frequencies within the stopband.

Alias-Free Bandwidth

Any signal that appears in the alias-free bandwidth of the NI PXIe-4330/4331 is not an aliased artifact of signals at a higher frequency. The alias-free bandwidth is defined by the ability of the filter to reject frequencies above the stopband frequency, and it is equal to the sample rate minus the stopband frequency.

Filter Group Delay

The digital filtering performed by the NI PXIe-4330/4331 produces a delay of many samples worth of time between when an event occurs on the input signal going into the NI PXIe-4330/4331 and when the data associated with that event is available at the output of the acquisition and filtering process. This delay is called the group delay.

In order to simplify the process of acquiring data from the NI PXIe-4330/4331 modules and correlating that data with data from other modules, the NI PXIe-4330/4331 compensates for this group delay in the following ways:

- The Sample Clock output from the NI PXIe-4330/4331 is generated at the point in time when the input signal is valid at the ADC input pins. When acquiring data, the NI PXIe-4330/4331 generates a Sample Clock, then waits for the data associated with that Sample Clock to be acquired, then returns that data. As a result, any other acquisitions timed with this Sample Clock line up with the data returned by the NI PXIe-4330/4331.
- Any triggers generated or received by the NI PXIe-4330/4331 are interpreted based on their relationship to the Sample Clock being generated. For example, a Start Trigger that starts an acquisition results in data from the next Sample Clock being returned as the first point in the acquisition. Refer to the *Triggering and Filter Delay* section for more details about how this affects analog trigger events.

- For any on-demand, software timed acquisition, the NI PXIe-4330/4331 waits for the group delay to elapse before returning the sample. As a result, the data returned aligns closely in time with when the data was requested. However, as a result, you must wait for the group delay to elapse before this sample is available.
- Similarly, for hardware timed acquisition at very low sample rates, you might notice that it takes several seconds for an acquisition to begin. This is because during start, the ADCs get reset and have to wait many samples before delta sigmas are operational. That time is dependent on the sample rate.

To improve the time it takes an acquisition to begin, select a higher sample rate.

Supported Data Rates

The NI PXIe-4330/4331 supports rates of 1 S/s to 100 S/s in 1 S/s increments. Rates beyond 100 S/s are supported in 100 S/s increments up to the maximum rate for the module.

Timing and Triggering

This section contains information about timing and triggering theory of operation.

Sample Clock Timebase

The ADCs require an oversample clock to drive the conversion. The oversample clock frequency is greater than the sample rate. On the NI PXIe-4330/4331 modules the oversample clock is produced from a DDS clock generation circuit. The DDS, in turn, is run from a 100 MHz reference clock. This 100 MHz reference clock can be supplied either by an onboard oscillator or by the PXI backplane 100 MHz clock. Multiple modules can be synchronized by selecting the PXI backplane 100 MHz clock as the reference clock source for all the modules. Refer to the *Reference Clock Synchronization* section for more information.

External Clock

The NI PXIe-4330/4331 ADCs cannot be clocked from external sources such as encoders or tachometers. However, signal processing features in the Sound and Vibration Measurement Suite often provide an excellent alternative to external clocking in encoder and tachometer applications. Visit `ni.com/soundandvibration` for more information about the Sound and Vibration Measurement Suite.

Digital Triggering

You can configure the NI PXIe-4330/4331 modules to start an acquisition in response to a digital trigger signal from one of the PXI Express backplane trigger lines. The trigger circuit can respond either to a rising or a falling edge. In addition, the trigger circuit provides a programmable filter useful for debouncing noisy trigger signals.

Analog Triggering

Analog triggering allows you to trigger your application based on an input signal and trigger level you define. You can configure the analog trigger circuitry to monitor any input channel acquiring data. Choosing an input channel as the trigger channel does not influence the input channel acquisition capabilities.

The analog trigger signal can be used as a reference trigger only. In a reference-triggered acquisition, you configure the module to acquire a certain number of pre-trigger samples and a certain number of post-trigger samples. The analog trigger on the NI PXIe-4330/4331 cannot be used as a start trigger. This restriction is a result of the way the module compensates for the filter group delay.

When using an analog reference trigger, the module first waits for the specified number of pre-trigger samples to be acquired. Once enough pre-trigger samples are acquired, the reference trigger will occur the next time the analog trigger condition is met. You also can route the resulting reference trigger event to the NI PXIe trigger bus to synchronize the triggering of other modules in the system.

During repetitive triggering on a waveform, you might observe jitter because of the uncertainty of where a trigger level falls compared to the actual digitized data. Although this trigger jitter is never greater than one sample period, it might be significant when the sample rate is only twice the bandwidth of interest. This jitter usually has no effect on data processing, and you can decrease this jitter by sampling at a higher rate.

You can use several analog triggering modes with the NI PXIe-4330/4331 modules, for instance analog edge, analog edge with hysteresis, and window triggering.

Analog Edge Triggering

For analog edge triggering, configure the module to detect a certain signal Level and slope, either rising or falling. Figure 2-20 shows an example of rising edge analog triggering. The analog comparison becomes true when the signal starts below Level and then crosses above Level.

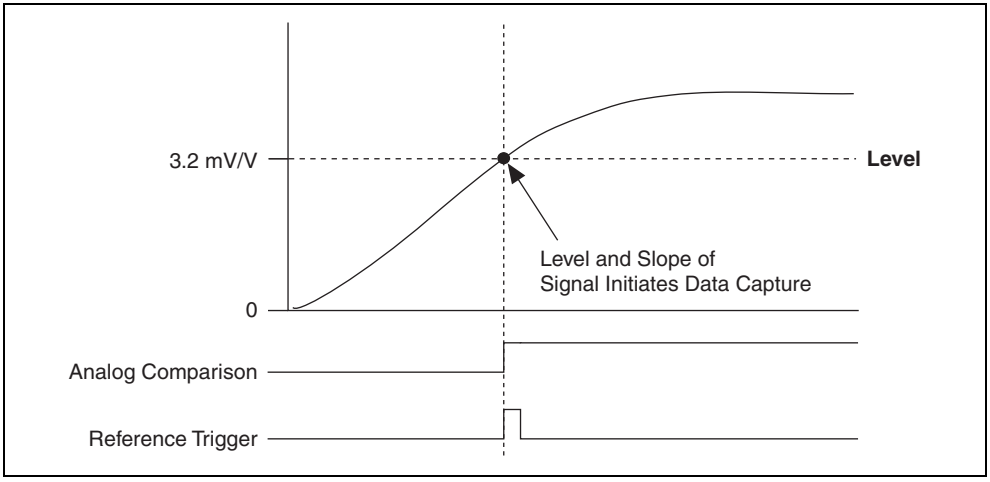


Figure 2-20. Analog Level Trigger on Rising Slope

Analog Edge Triggering With Hysteresis

When you add hysteresis to analog edge triggering, you add a window above or below the trigger level. This triggering mode often is used to reduce false triggering due to noise or jitter in the signal. For example, if you add a hysteresis of 1 mV/V to the example in Figure 2-20, which uses a level of 3.2 mV/V, the signal must start at or drop below 2.2 mV/V to arm the trigger. The analog comparison becomes true when the signal rises above 3.2 mV/V and becomes false when it falls below 2.2 mV/V, as shown in Figure 2-21.

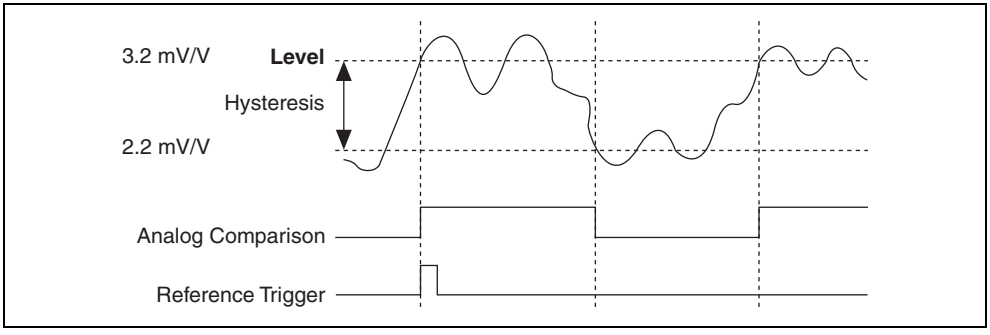


Figure 2-21. Analog Edge Triggering with Hysteresis on Rising Slope

When using hysteresis with a falling slope, the trigger is armed when the signal starts above Level plus the hysteresis value and asserts when the signal crosses below Level. For example, if you add a hysteresis of 1 mV/V to a level of 3.2 mV/V, the signal must start at or rise above 4.2 mV/V to arm the trigger. The analog comparison becomes true as the signal falls below 3.2 mV/V and becomes false when it rises above 4.2 mV/V, as shown in Figure 2-22.

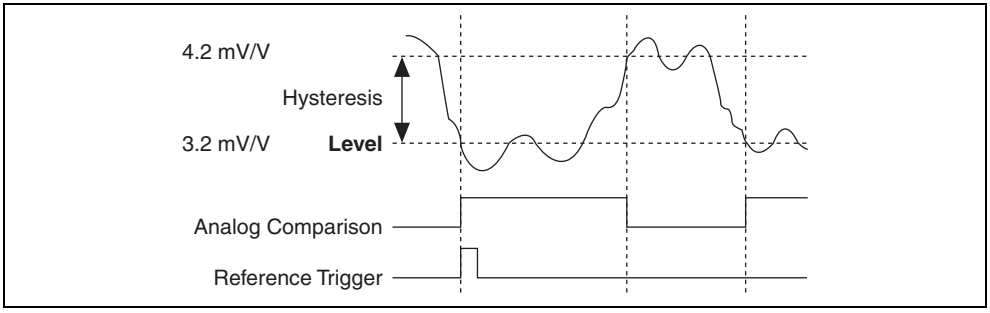


Figure 2-22. Analog Edge Triggering with Hysteresis on Falling Slope

Window Triggering

A window trigger occurs when an analog signal either passes into (enters) or passes out of (leaves) a window defined by two levels. Specify the levels by setting a value for the top and bottom window boundaries. Figure 2-23 demonstrates a trigger that acquires data when the signal enters the window. You can also program the trigger circuit to acquire data when the signal leaves the window.

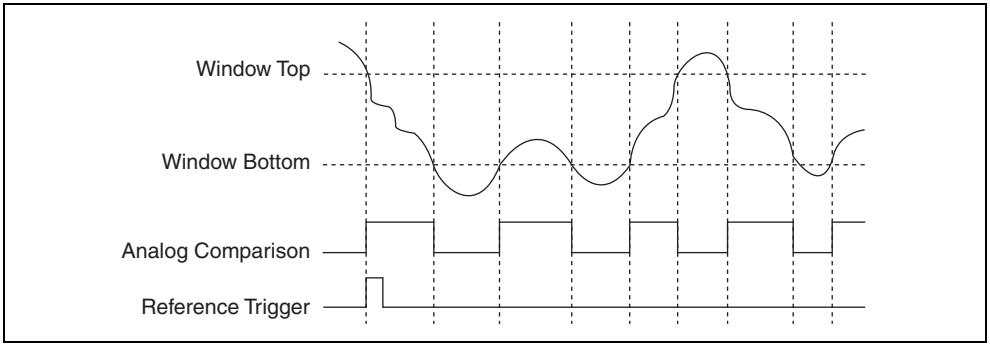


Figure 2-23. Window Triggering

Triggering and Filter Delay

The NI PXIe-4330/4331 can use a digital trigger signal from the backplane as either a start trigger initiating an acquisition, or a reference trigger in the middle of an acquisition. The NI PXIe-4330/4331 can also generate an analog trigger event from its digitized ADC data. As a result of the way the NI PXIe-4330/4331 modules adjust for its digital filter group delay, analog triggers can only act as reference triggers.

In all cases, the NI PXIe-4330/4331 interprets triggers based on where they occur in time. The hardware automatically compensates for its group delay such that data from this module will line up closely in time with the occurrence of the trigger event. However, the group delay affects how long it takes to receive data after the trigger event. For example, after a digital start trigger, you can not read data for the first sample in software until the filter group delay has elapsed. Refer to the *NI PXIe-4330/4331 Specifications* document for details regarding the group delay at different sample rates.

Synchronization

Some applications require tight synchronization between input and output operations on multiple modules. Synchronization is important to minimize skew between channels or to eliminate clock drift between modules in long-duration operations. You can synchronize the analog input operations on two or more NI PXIe-4330/4331 modules to extend the channel count for your measurements. In addition, the NI PXIe-4330/4331 can synchronize with certain other DSA modules, such as the NI PXIe-449x modules, using Reference Clock Synchronization.

You can also synchronize modules that support external timing to the NI PXIe-4330/4331 by routing the SampleClock output from the NI PXIe-4330/4331 to the external device. The SampleClock toggles every time that the NI PXIe-4330/4331 acquires a sample, and it toggles at the point in time that the input signal was valid at the NI PXIe-4330/4331 ADC input pins. This means that you can synchronize the NI PXIe-4330/4331 to any other module that can trigger its acquisitions using the NI PXIe-4330/4331 SampleClock.

Reference Clock Synchronization

With reference clock synchronization, master and slave modules generate their ADC oversample clock from the shared 100 MHz reference clock from the PXIe backplane (PXIe_CLK100). The backplane supplies an identical copy of this clock to each peripheral slot. In addition, multiple chassis can be synchronized by using a timing and synchronization board to lock the 100 MHz clock across chassis.

When you acquire data from multiple modules within the same NI-DAQmx task, NI-DAQmx will automatically handle all of the Reference Clock Synchronization details required to synchronize the modules within the task. This is known as a Multi-Device Task.

To perform Reference Clock Synchronization when using multiple NI-DAQmx tasks that are acquiring at the same rate, complete the following steps to synchronize the hardware.

1. Specify PXIe_CLK100 as the reference clock source for all modules to force all the modules to lock to the reference clock on the PXIe chassis.
2. Choose an arbitrary NI PXIe-4330/4331 master module to issue a sync pulse on one of the PXIe Trigger lines. The sync pulse resets the ADCs and oversample clocks, phase aligning all the clocks in the system to within nanoseconds.
3. Configure the rest of the modules in your system to receive their sync pulse from the sync pulse master module. This will ensure all ADCs are running in lockstep.
4. Choose one module to be the start trigger master. This does not have to be the same module you chose in step 3, depending on your application.
5. Configure the rest of the modules in your system to receive their start trigger from the start trigger master module. This ensures that all modules will begin returning data on the same sample.
6. Set the synchronization type of the Start Trigger slaves at **DAQmx Trigger»Advanced» Synchronization» Synchronization Type** to Slave and that of the Master to Master. Also query **DAQmx Timing»More»Synchronization Pulse»Synchronization Time** on all modules being synchronized, choose the maximum value and set that as the **DAQmx Timing»More»Synchronization Pulse»Minimum Delay To Start** on all modules.
7. Commit all of the sync pulse slave module tasks using the DAQmxTaskControl VI/Function. This sets them up to expect the sync pulse from the master.
8. Commit the sync pulse master module task using the DAQmxTaskControl VI/Function. This will issue the sync pulse.
9. Start all of the start trigger slave module tasks. This sets them up to expect the start trigger from the master.
10. Start the start trigger master module task. You can now acquire data.

Consider using a Multi-Device task when synchronizing multiple devices at the same rate. Refer to Multi-Device Synch-Analog Input-Cont Acq-Multi Rate-PXIe-433x VI for an example of how to synchronize when acquiring at different rates.

Consider the following caveat to using Reference Clock synchronization:

- The NI PXIe-4330/4331 automatically compensates for its filter group delay. However, some other device families do not compensate for their filter delay. In this case, you might need to compensate for group delay in the waveforms when you synchronize between device families.

TEDS

The NI PXIe-4330/4331 supports communicating with Transducer Electronic Data Sheet (TEDS)-enabled sensors (IEEE 1451.4 Class 2). TEDS-enabled sensors carry a built-in, self-identification EEPROM containing a table of parameters and sensor information. This allows your data acquisition system to automatically detect and configure the sensors.

TEDS contains information about the sensor such as calibration, sensitivity, and manufacturer information. This information is accessible in Measurement & Automation Explorer (MAX), VIs in LabVIEW, or by calling the equivalent function calls in a text-based ADE.

For more information about TEDS plug and play sensors, refer to `ni.com/pnp`.

Configuring and Using TEDS in Software

To manually configure TEDS in MAX, right click on the NI PXIe-4330/4331 module within the Configuration tree. Then select **Configure TEDS** from the pop-up menu.

To programmatically configure TEDS, call the DAQmx Configure TEDS VI.

Accessory Auto-Detection

NI SC Express modules automatically detect compatible accessories or terminal blocks. The RSVD pins on the I/O connector provide power to the accessories as well as digital communication lines. This allows software to detect when accessories are inserted or removed. In addition, software can automatically identify the specific terminal block as well as access any calibration or scaling information associated with the terminal block.

Measurement & Automation Explorer (MAX) allows you to see what accessories are currently connected to your module. In MAX, expand **Devices and Interfaces** and locate your module. If a terminal block is connected to your module, it will be displayed beneath the module. Unsupported terminal blocks appear in MAX with an X next to them.

NI-DAQmx property nodes can be used to programmatically access information about connected accessories in your application. Refer to the *NI-DAQmx Help* for documentation about programmatically accessing accessory status. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**.

3

NI SC Express Considerations

This chapter details the clock and trigger functionality available through the PXI Express chassis.

NI SC Express Clock and Trigger Signals

PXIe_CLK100

PXIe_CLK100 is a common, low-skew 100 MHz reference clock used for synchronization of multiple modules in a PXI Express measurement or control system. The NI PXIe backplane is responsible for generating PXIe_CLK100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXIe_SYNC100

PXIe_SYNC100 is a common, low-skew 10 MHz reference clock with a 10% duty cycle for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe_SYNC100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXI_CLK10

PXI_CLK10 is a common, low-skew 10 MHz reference clock for synchronization of multiple modules in a PXI measurement or control system. The PXI backplane is responsible for generating PXI_CLK10 independently to each peripheral slot in a PXI chassis.

Note PXI_CLK10 cannot be used as a reference clock for SC Express modules.

PXI Triggers

A PXI chassis provides eight bused trigger lines to each module in a system. Triggers may be passed from one module to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. Triggers can be used to synchronize the operation of several different PXI peripheral modules.

On SC Express modules, the eight PXI trigger signals are synonymous with RTSI <0..7>. In a PXI chassis with more than eight slots, the PXI trigger lines may be divided into multiple independent buses. Refer to the documentation for your chassis for details.

PXI_STAR Trigger

In a PXI Express system, the Star Trigger bus implements a dedicated trigger line between the system timing slot and the other peripheral slots. The Star Trigger can be used to synchronize multiple modules or to share a common trigger signal among modules.

A system timing controller can be installed in the system timing slot to provide trigger signals to other peripheral modules. Systems that do not require this functionality can install any standard peripheral module in this system timing slot.

An SC Express module receives the Star Trigger signal (PXI_STAR) from a System timing controller. PXI_STAR can be used as a trigger signal for input operations.

An SC Express module is not a System timing controller. An SC Express module can be used in the system timing slot of a PXI system, but the system will not be able to use the Star Trigger feature.

PXIe_DSTAR<A..C>

PXI Express devices can provide high-quality and high-frequency point-to-point connections between each slot and a system timing slot. These connections come in the form of three low-voltage differential star triggers that route between a PXI Express system timing controller and a peripheral device. Using multiple connections simplifies the creation of applications because of the increased routing capabilities.

Table 3-1 describes the three differential star (DSTAR) lines and how they are used.

Table 3-1. PXIe_DSTAR Line Descriptions

Trigger Line	Purpose
PXIe_DSTARA	Distributes high-speed, high-quality clock signals from the system timing slot to the peripherals (input).
PXIe_DSTARB	Distributes high-speed, high-quality trigger signals from the system timing slot to the peripherals (input).
PXIe_DSTARC	Sends high-speed, high-quality trigger or clock signals from the peripherals to the system timing slot (output).

The DSTAR lines are only available for PXI Express devices when used with a PXI Express system timing module. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

Trigger Filters

You can enable a programmable debouncing filter on each PXI_Trig, PXIe_DSTAR, or PXI_STAR signal. When the filters are enabled, your module samples the input on each rising edge of a filter clock. This filter clock is generated using the onboard oscillator.

The following example explains how the filter works for low to high transitions of the input signal. High-to-low transitions work similarly.

Assume that an input terminal has been low for a long time. The input terminal then changes from low to high, but glitches several times. When the filter clock has sampled the signal high on N consecutive edges, the low to high transition is propagated to the rest of the circuit. The value of N depends on the filter setting. Refer to Table 3-2.

Table 3-2. Filters

Filter Setting	Filter Clock	N (Filter Clocks Needed to Pass Signal)	Pulse Width Guaranteed to Pass Filter	Pulse Width Guaranteed to Not Pass Filter
None	—	—	—	—
90 ns (short)	100 MHz	9	90 ns	80 ns
5.12 µs (medium)	100 MHz	512	5.12 µs	5.11 µs
2.56 ms (high)	100 kHz	256	2.56 ms	2.55 ms
Custom	User Configurable	N	N/timebase	(N – 2)/timebase

The filter settling for each input can be configured independently. At power on, the filters are disabled.

Enabling filters introduces jitter on the input signal. The maximum jitter is one period of the timebase.

These filters work by rejecting any pulse shorter than the specified filter setting. For example, a 5.12 µs filter will reject any pulses shorter than 5.12 µs. The trigger filters can be used to prevent false triggers from occurring in cases where the trigger signal is noisy or glitchy.

A

Offset Nulling (Bridge Balancing)

When you install a bridge-based sensor, the bridge probably will not output exactly 0 V when not under load. Slight variations in resistance among the bridge legs generate some nonzero initial offset voltage. Use the DAQmx Perform Bridge Offset Nulling Calibration VI/function or the DAQ Assistant to perform an offset nulling calibration, which will apply software compensation for the bridge.

NI-DAQmx will measure the bridge while not under load, and then use this measurement as the initial bridge voltage when scaling readings from the bridge. This method is simple, fast, and requires no manual adjustments. The disadvantage of the software compensation method (in contrast to hardware compensation) is that software compensation does not physically remove the offset of the bridge. If the offset is large enough, it limits the amplifier gain you can apply to the output voltage, thus limiting the dynamic range of the measurement. The NI PXIe-4330/4331 does not have any internal hardware nulling circuitry, however, its input range is sufficiently wide so that the inputs will not saturate even with a relatively large initial bridge offset.

B

Technical Support and Professional Services

Visit the following sections of the award-winning National Instruments Web site at ni.com for technical support and professional services:

- **Support**—Technical support at ni.com/support includes the following resources:
  - **Self-Help Technical Resources**—For answers and solutions, visit ni.com/support for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at ni.com/forums. NI Applications Engineers make sure every question submitted online receives an answer.
  - **Standard Service Program Membership**—This program entitles members to direct access to NI Applications Engineers via phone and email for one-to-one technical support as well as exclusive access to on demand training modules via the Services Resource Center. NI offers complementary membership for a full year after purchase, after which you may renew to continue your benefits.

    For information about other technical support options in your area, visit ni.com/services, or contact your local office at ni.com/contact.
- **Training and Certification**—Visit ni.com/training for self-paced training, eLearning virtual classrooms, interactive CDs, and Certification program information. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.
- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification.
- **Calibration Certificate**—If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.

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this manual. You also can visit the Worldwide Offices section of `ni.com/niglobal` to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.